Code: 20CS3301, 20IT3301

II B.Tech - I Semester – Regular / Supplementary Examinations
DECEMBER 2023

FUNDAMENTALS OF DIGITAL LOGIC DESIGN
(Common for CSE, IT)

Duration: 3 hours   Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level   CO – Course Outcome

			BL	CO	Max. Marks
		UNIT-I			
1	a)	Convert the following base conversions using Number System. i. $(365.24)_{10}$ to $(\ ?\ )_2$ ii. $(333.45)_8$ to $(?)_2$ iii. $(A\,B\,7.D)_{16}$ to $(?)_8$	L2	CO1	7 M
	b)	i. Convert the $(1110001.10001)_2$ binary number to decimal, hexadecimal and octal numbers. ii. Subtract $(11111)_2$ from $(10101)_2$ using 2's complement method.	L2	CO1	7 M
		OR			
2	a)	Show the Gray code for the following decimal numbers. i. $(73)_{10}$ ii. $(77)_{10}$	L2	CO1	7 M

	b)	Show the Excess 3 code for the following decimal numbers. i. $(1111)_{10}$ ii. $(11)_{16}$	L2	CO1	7 M

UNIT-II					
3	a)	Using Boolean laws verify the following equation. $(X + \overline{Y} + XY)(X + \overline{Y})\overline{X}Y = 0$	L2	CO2	7 M
	b)	Using Boolean laws prove that $xy + \overline{x} + yz = \overline{x} + y$	L2	CO2	7 M

OR					
4	a)	Minimize the expression using K-map. $Y = \overline{A}B\overline{C}\overline{D} + \overline{A}B\overline{C}D + AB\overline{C}\overline{D} + AB\overline{C}D + A\overline{B}\overline{C}D + \overline{A}\,\overline{B}CD$	L3	CO2	7 M
	b)	Obtain the simplified expression in product of sums using K-map and draw the circuit diagram. $f(A,B,C,D) = \pi(2,7, 8, 9,10,12)$	L3	CO2	7 M

UNIT-III					
5	a)	Design a BCD code to excess-3 code converter and draw the logic diagram.	L3	CO3	7 M
	b)	Design a full-subtractor with two half-subtractors and an OR gate.	L3	CO3	7 M

OR					
6	a)	Draw the truth table and the circuit for 3:8 decoder and explain.	L3	CO3	7 M
	b)	Show the truth table of 4-bit priority encoder and design the logical circuit of the 4-bit priority encoder.	L3	CO3	7 M

		UNIT-IV			
7	a)	Design the conversion logic to convert SR flip-flop into T flip-flop.	L4	CO3	7 M
	b)	Compare combinational and sequential circuits.	L2	CO4	7 M
		OR			
8	a)	Design the conversion logic to convert JK flip-flop into D flip-flop.	L4	CO4	7 M
	b)	Show the excitation table of the following flip-flops. i. JK flip-flop ii D flip-flop	L2	CO3	7 M
		UNIT-V			
9	a)	Design a BCD ripple counter using JK flip-flops.	L3	CO3	7 M
	b)	Design a three bit bi-directional shift register that shifts the bits to left when a control variable $E = 0$ and shifts the bits to right when $E = 1$ using D flip-flops.	L4	CO3	7 M
		OR			
10	a)	Design a 4-bit Johnson counter.	L4	CO4	7 M
	b)	Compare and contrast the synchronous counters with the asynchronous counters.	L2	CO3	7 M